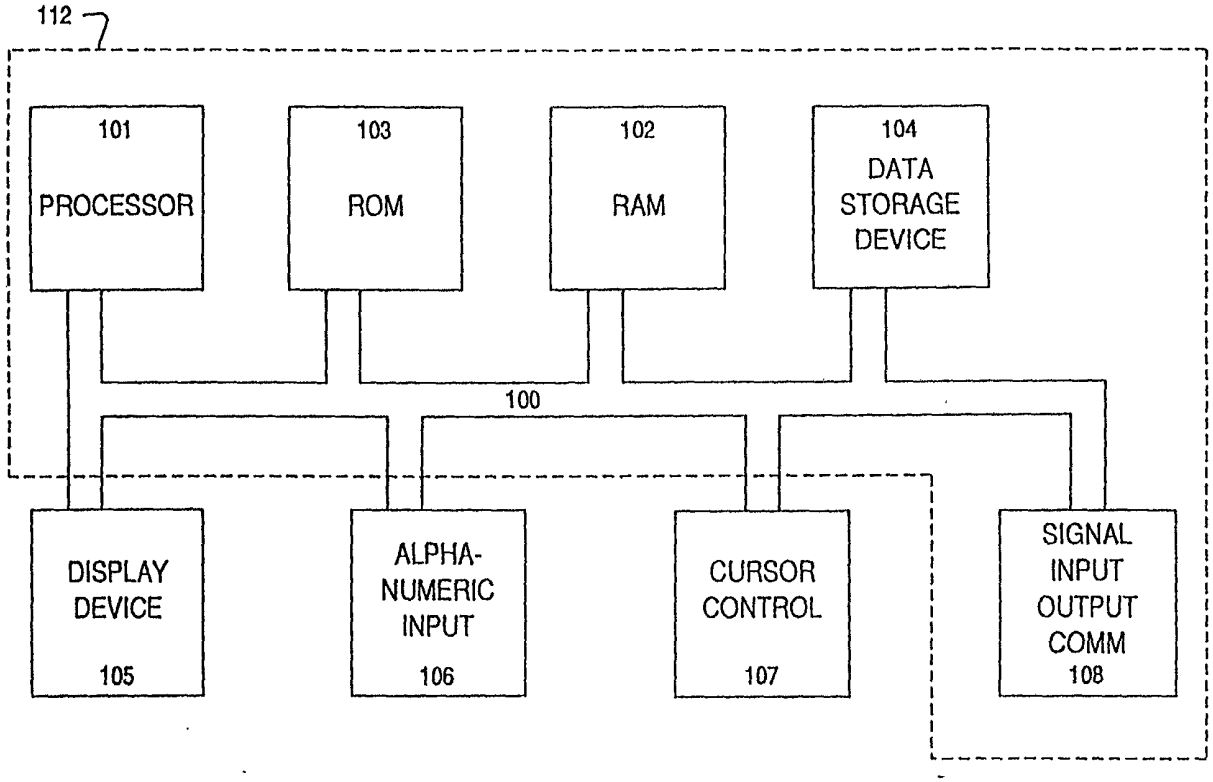

Figure 1

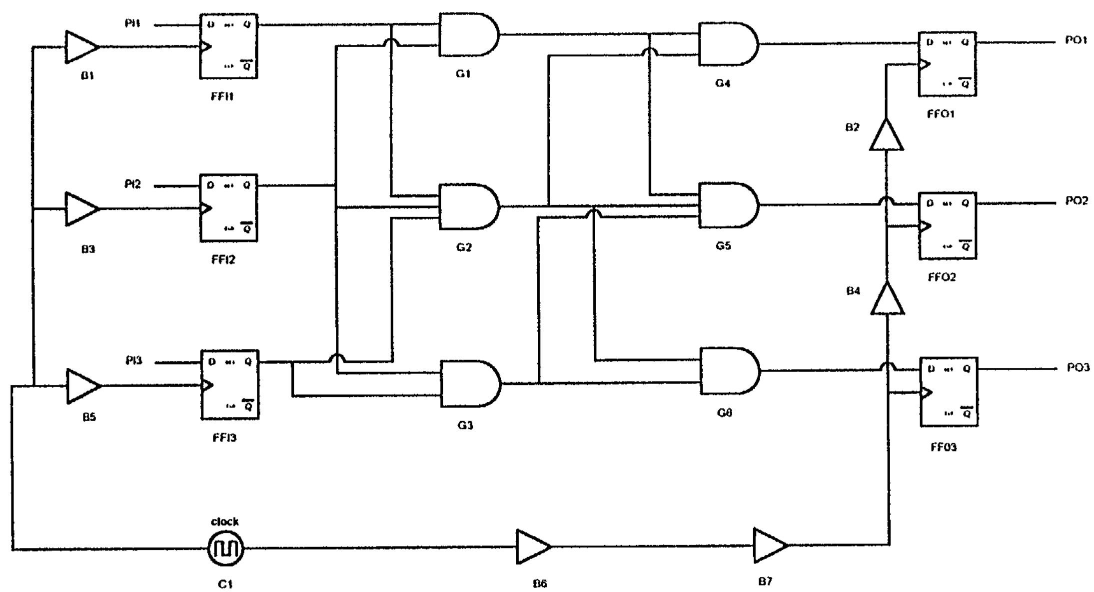
PI1
PI2
PI3
B1
B3
B5
FFI1
FFI2
FFI3
D
Q
G1
G2
G3
G4
G5
G6
B2
B4
FFO1
FFO2
FFO3
PO1
PO2
PO3
clock
C1
B6
B7

FIGURE 2A

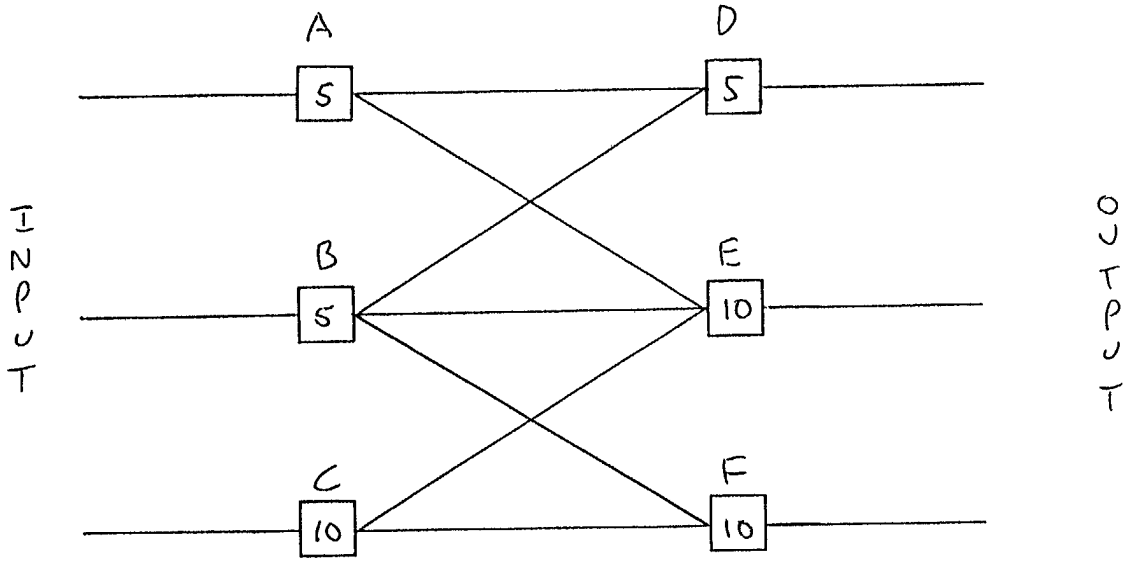

Figure 2B

Forward Delay Sums

A	B	C
(5)	(5)	(10)
	5	

D	E	F
(10)	(15)	(15)
10	15	20
	20	

Figure 3

T_{qi}	T_{sj}	T_{hj}	HOLD TIME CONSTRAINT	MINIMUM FORWARD DELAY SUM	MAXIMUM FORWARD DELAY SUM	SETUP TIME CONSTRAINT	OUTPUT NODE
2	12	9	7	10	10	26	D
2	3	8	6	15	20	35	E
2	19	10	8	15	20	19	F

Clock Period = 40

Setup Time Constraint = Clock Period - T_{qi} - T_{sj}

Hold Time Constraint = T_{hj} - T_{qi}

FIGURE 4

STAEDTLER® No. 937 811E Engineer's Computation Pad

Reverse Delay Differences

D	E	F
21	25	9

A	B	C
16	16	15
20	20	-1
	4	

Figure 5

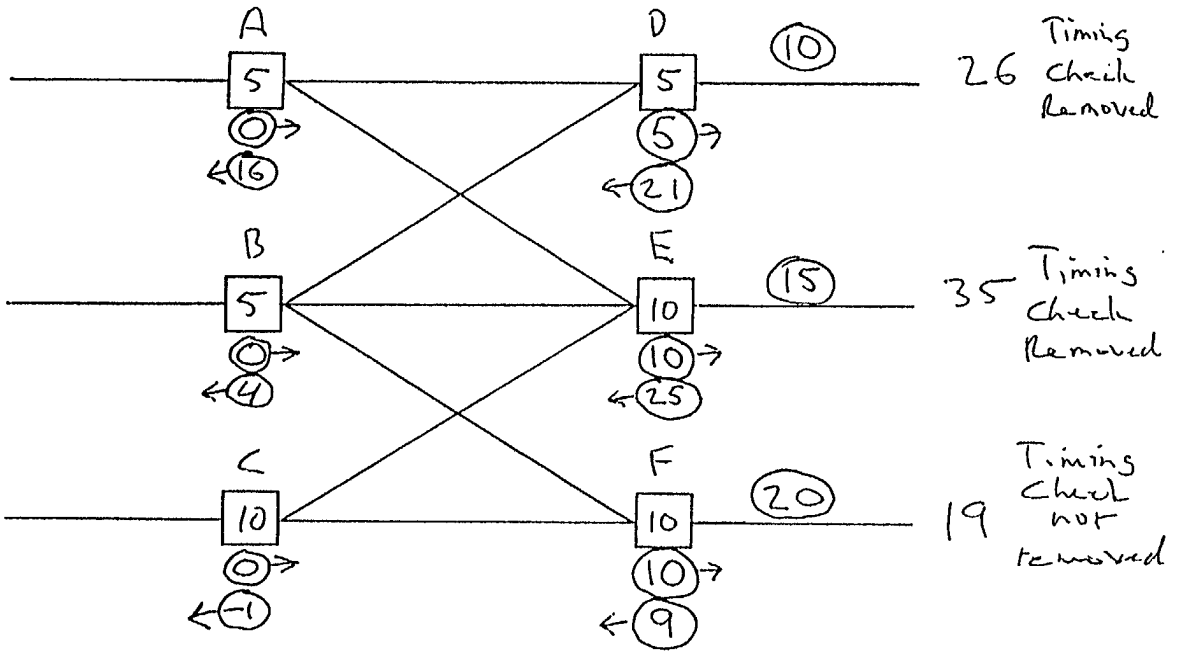

Figure 6

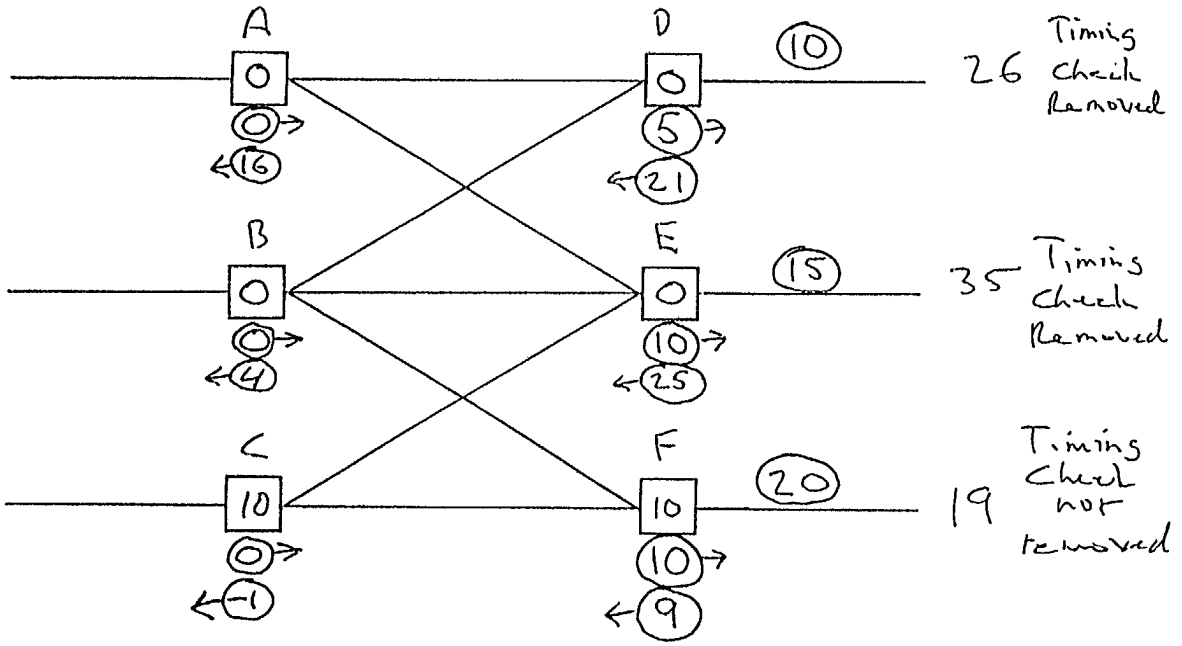

Figure 7A

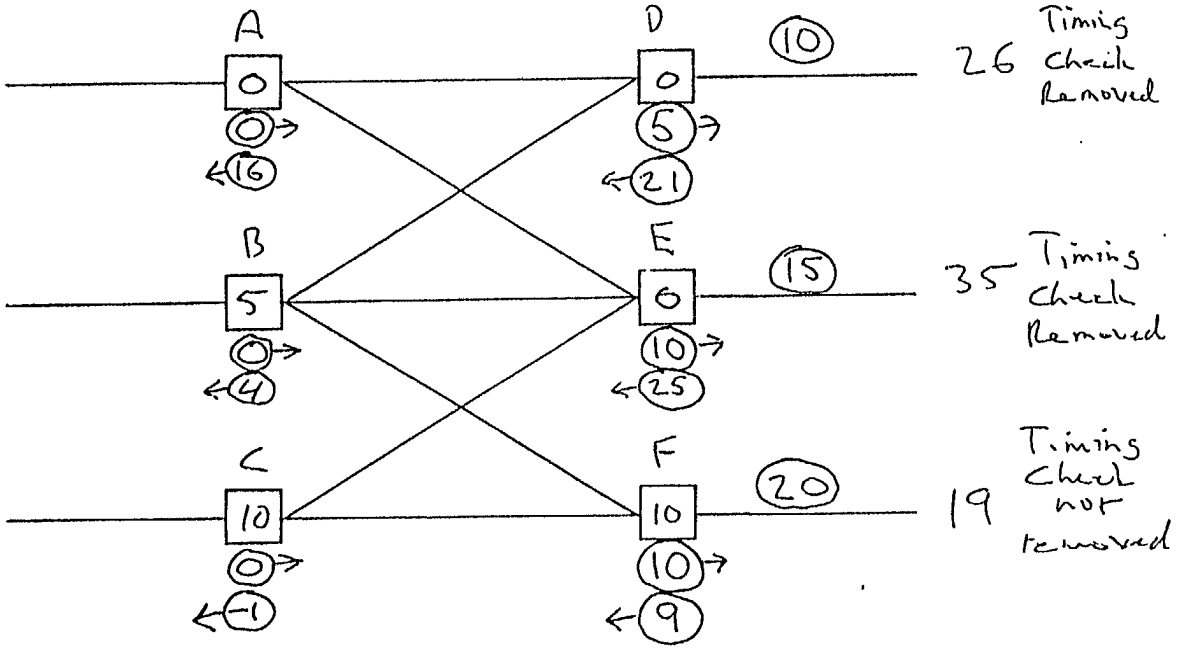

Figure 7B

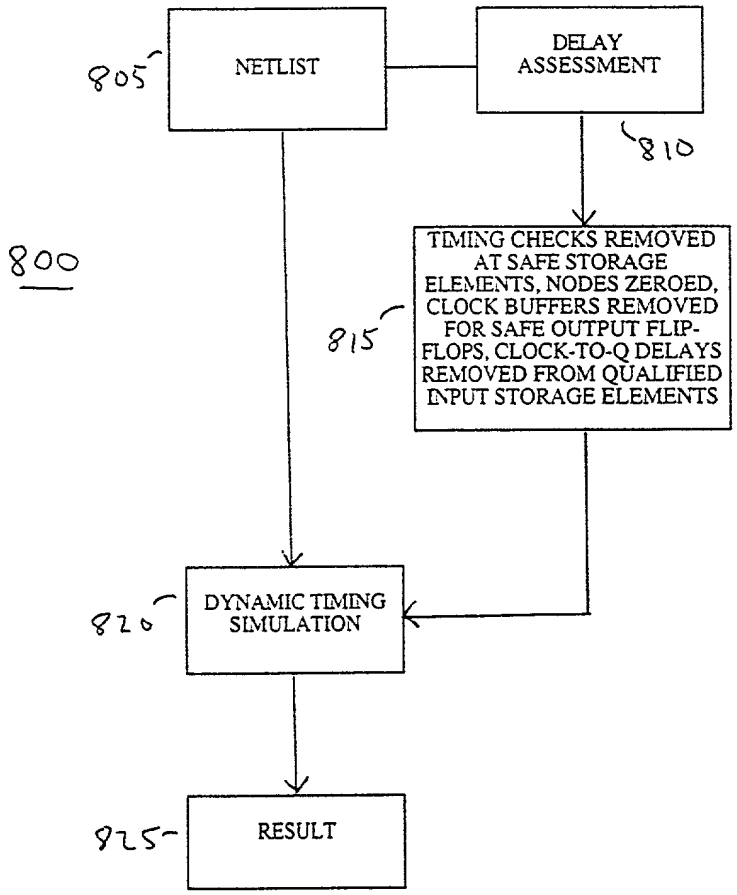
800
805
NETLIST
DELAY ASSESSMENT
810
815
TIMING CHECKS REMOVED AT SAFE STORAGE ELEMENTS, NODES ZEROED, CLOCK BUFFERS REMOVED FOR SAFE OUTPUT FLIP-FLOPS, CLOCK-TO-Q DELAYS REMOVED FROM QUALIFIED INPUT STORAGE ELEMENTS
820
DYNAMIC TIMING SIMULATION
825
RESULT

FIGURE 8

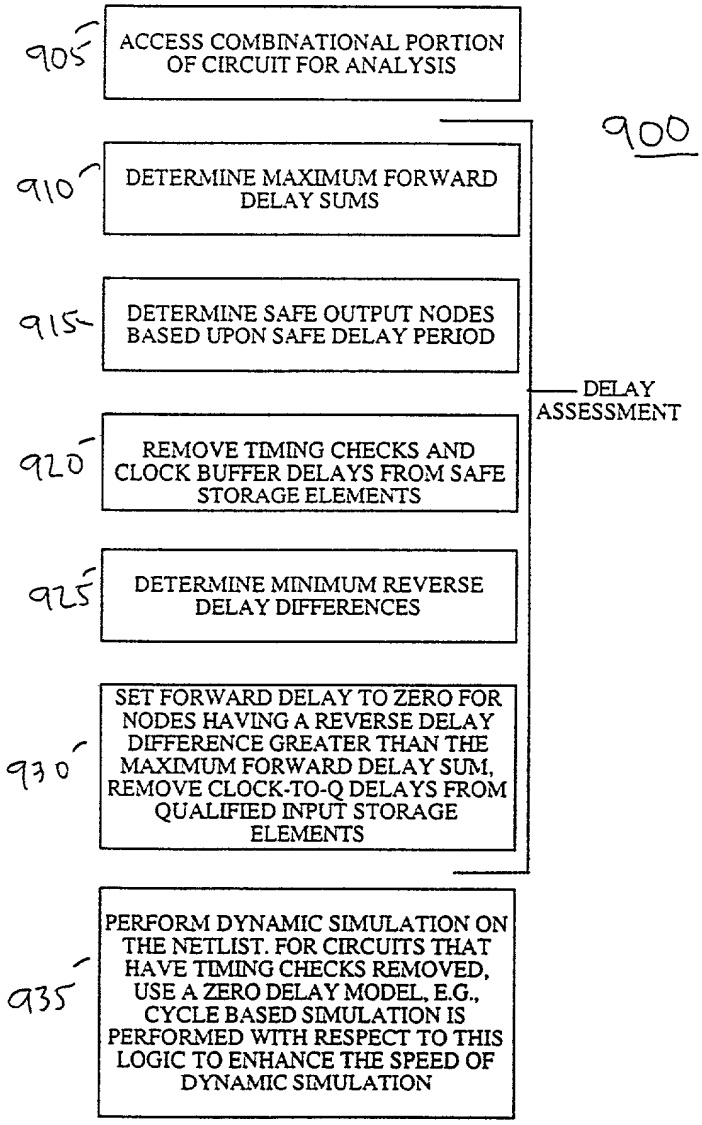
905
ACCESS COMBINATIONAL PORTION OF CIRCUIT FOR ANALYSIS
900
910
DETERMINE MAXIMUM FORWARD DELAY SUMS
915
DETERMINE SAFE OUTPUT NODES BASED UPON SAFE DELAY PERIOD
DELAY ASSESSMENT
920
REMOVE TIMING CHECKS AND CLOCK BUFFER DELAYS FROM SAFE STORAGE ELEMENTS
925
DETERMINE MINIMUM REVERSE DELAY DIFFERENCES
930
SET FORWARD DELAY TO ZERO FOR NODES HAVING A REVERSE DELAY DIFFERENCE GREATER THAN THE MAXIMUM FORWARD DELAY SUM, REMOVE CLOCK-TO-Q DELAYS FROM QUALIFIED INPUT STORAGE ELEMENTS
935
PERFORM DYNAMIC SIMULATION ON THE NETLIST. FOR CIRCUITS THAT HAVE TIMING CHECKS REMOVED, USE A ZERO DELAY MODEL, E.G., CYCLE BASED SIMULATION IS PERFORMED WITH RESPECT TO THIS LOGIC TO ENHANCE THE SPEED OF DYNAMIC SIMULATION

FIGURE 9